Figure 8A is a side view of a positive nanometer-pitched feature formed in a micrometer-pitched channel using edge definition lithography according to an embodiment of the present invention;

Figure 8B is a side view of a positive nanometer-pitched feature formed in a micrometer-pitched channel using edge definition lithography according to an embodiment of the present invention;

Figure 8C is a side view of a negative nanometer-pitched feature formed in a micrometer-scale channel according to an embodiment of the present invention;

Figure 8D is a side view of a negative nanometer-pitched feature formed on a micrometer-scale mesa according to an embodiment of the present invention;

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Figure 9A-9E are side views of a nanometer-pitched HFETs or MESFETs formed using edge definition lithography according to an embodiment of the present invention; and

Figure 10A is a side view of a heterojunction biopolar junction transistor formed using edge definition lithography according to an embodiment of the present invention;

Figure 10B is a side view of a heterojunction bipolar junction transistor formed using edge definition lithography according to an embodiment of the present invention; and

Figure 10C is a perspective view of a heterojunction bipolar junction transistor formed using edge definition lithography according to an embodiment of the present invention.

Detailed Description of the Invention

As stated above, the present invention includes methods and systems for multiperiod edge definition lithography. Figures 1A through 1I illustrate an exemplary multiperiod edge definition lithography method according to an embodiment of the present invention. Referring to Figure 1A, a block feature or mesa **100** is defined on a substrate **102** using standard photolithographic techniques. The spatial dimensions of mesa **100** may be consistent with the